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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/787,369	JEON ET AL.
	Examiner	Art Unit
	Alexander Sofocleous	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 and 18-20 is/are rejected.

7)☒ Claim(s) ~~1-23~~ 7-17, 21-23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 February 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 26, 2004.

2. Claims 1-23 are pending in the case. Claim 1, 7, 18, and 21 are independent claims.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

4. The drawings are objected to because of minor discrepancies between the drawings and the specification. The specification indicates that step 110 of Figure 2 depends on if WEB is logic low (page 8, line 22); while Figure 2 step 110 depends on if CEB is logic low. Figure 5 has a similar discrepancy. Examiner assumes that the specification is correct and the applicant intended for the second step of the method for writing data to depend on if WEB is logic low.

The specification indicates that step 350 of Figure 3 checks for activation of DET; while Figure 3 shows step 350 checking activation of WL1. Figure 6 has a similar discrepancy (Fig. 6 [450]). Examiner assumes that the specification is correct and the applicant intended for step 350 of Fig. 3 to check for activation of DET.

It is suggested that applicant carefully review the drawings with respect to the specification and make appropriate corrections accordingly.

Figure 4 refers to a bit region in the OTP region as a "parity bit region." However, this region, as defined by the specification (page 13, line 2-3), is more commonly referred to as a "lock bit region" (see specification objection below). Examiner suggests re-labeling this region in Figure 4 as "lock bit region," and updating Figure 5 and Figure 6 to reflect this change.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities: the term "write enable signal" is used to define (WEB) and (WDEN). Although applicant indicates which "write enable signal" is being referred to by use of (WEB) or (WDEN), Examiner recommends that applicant refer to WEB as the "write enable signal" and refer to WDEN as the "write driver enable signal" for clarity purposes. Hence, Examiner suggests changing all instances of "write enable signal WDEN" to -- write drive enable signal WDEN --.

Applicant also refers to a "parity bit" (see page 13, line 2-3), which is more commonly known in the art of one-time programmable memories as a "lock bit." A parity bit is defined as a bit determining an even or odd number of active bits (logic high or logic low) in a data (see definition of parity bit from TechWeb with respect to definition of parity checking from TechWeb). Applicant indicates that the parity bit region (Fig. 4 [parity bit region]) depends on whether the data in the OTP has been completely programmed, and not on the odd or even number of active bits. Examiner suggests modifying the specification, figures, and claims to reflect the more commonly known term: "lock bit."

Appropriate correction is required.

Claim Objections

6. **Claims 1, 3, 7, 10, and 11** are objected to because of the following informalities: the write driver enable signal is referred to as "write enable signal," which conflicts with the specification and drawings. Examiner suggests that

applicant replace "write enable signal" with "write driver enable signal" because the "write enable signal" (Fig. 1, Fig. 4 [WEB]) is independent of the data output. Claims 2, 4-6, 8-9, and 12-17 are objected to as being dependent on an objected base claim.

Claims 7, 9, 10, 16, 17, and 21 are objected to because of the following informalities: consistent with Examiner's statements in paragraph 4 and 5, it is suggested that the applicant replace "parity bit" with "lock bit" where such appears in the claims. A feature that determines whether a memory region is one-time programmable is more commonly known in the art as a "lock bit." Claims 8, 11-15, 18-20, 22, and 23 are objected to as being dependent on an objected base claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1, 3, 4, 6, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Fasoli (U.S. Patent 6,490,197 B1).**

Regarding independent claim 1, Fasoli shows a nonvolatile semiconductor memory device (Fig. 2 [1]) that comprises a nonvolatile memory cell array (Fig. 2 [2]) having a modify protected region, or one-time programming region (Fig. 2 [3a]; see column 5, lines 53-57), accessed in response to a first decoding signal (see Fig. 2 [connection from 7 and 2]) and a normal region (Fig. 2 [3]) accessed in response to a second decoding signal (see Fig. 2 [connection from 7 and 2])) wherein the nonvolatile memory cell array performs a read and a write operation (column 5, lines 61-65).

Fasoli shows a data write circuit (Fig. 2 [24]) writes data in the nonvolatile memory cell array (Fig. 2 [2]) in response to a write enable signal (see Fig. 2 [connection from 23 and 24]) during the write operation.

Fasoli shows a data read circuit (Fig. 2 [9]) reads data output from the nonvolatile memory cell array (Fig. 2 [2]) in response to a sense amplifier enable signal (see Fig. 2 [connection from 23 and 9]) during the read operation.

Fasoli shows a controller (Fig. 2 [23]) for activating the sense amplifier enable signal (see Fig. 2 [connection from 23 and 9]) when the first decoding signal (see Fig. 2 [connection from 7 and 2]) is generated and comparing the data output (Fig. 2 [20a]) from the data read circuit (Fig. 2 [9]) to generate the write enable signal (see Fig. 2 [connection from 23 and 24]) during the write operation (see Fig. 2 [connection from 9 to 23]; see column 6, lines 36-50).

As per **independent claim 18**, it encompasses the same scope of invention as to that of claim 1 except it drafts in method format instead of

apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 3, Fasoli shows the controller (Fig. 2 [23]) that determines if a memory sector is "modify protected," or one time programmable, based on the data output of a cell in that sector (column 6, line 36-39). Although not specifically disclosed or shown, it is implicit that the controller has a built-in comparison means, or program detecting circuit, for the data output and accompanying internal comparison detecting signal that is controlled by a control signal internal to the controller.

Fasoli shows the controller (Fig. 2 [23]), which implicitly has a control means. Another connected controller (Fig. 2 [22]) has connected inputs (Fig. 2 [control inputs]) for the purpose of selecting a memory modifying operation, or an operation mode (column 6, lines 27-29). Therefore, it is indicative that such inputs include a mode selection signal, or read/modify signal, or specific mode signal.

When a read signal is applied to the controller, the comparison of the data output with respect to whether the memory region is one-time programmable or multiple-time programmable is not required (see column 4, lines 43-59). A read operation, with respect to the limitations discussed above, is performed in the same fashion on a one-time programmable region as a multiple-programmable region. Therefore, the control signal implicitly internal to the controller is deactivated when the read signal is applied.

When a modify signal is applied on the one-time programmable memory (Fig. 2 [3a]), in response to the first decoding signal, the control signal is activated and the sense amplifier enable signal is activated. The write enable signal is activated when the comparison detecting signal (as discussed above) is activated during a write operation (column 6, lines 36-39).

Regarding dependent claim 4, Fasoli shows that the controller (Fig. 2 [23]), which includes implicit control means, activates the sense amplifier enable signal (see Fig. 2 [connection from 23 and 9]) during the read operation.

Regarding dependent claim 5, for examination purposes, the subject matter in parentheticals is not given patentable weight nor is it considered to further limit the scope of the invention. Fasoli discloses that the controller compares data from the memory cell (Fig. 2 [20a]) which indicates that a program detecting circuit is enabled when the control signal is activated and is disabled when the control signal is inactivated (as discussed above). Fasoli is flexible with respect to the number of cells used in determining whether the nonvolatile region is one-time programmable (see column 35, line 35, 20a is references as "memory cells"; see column 6, line 39, 20a is referenced as "memory cell"). In the instance that one cell is used for this determination, the cell will hold one of two values: logic "high," or logic "low." Fasoli is silent with respect to whether either logic "high" or logic "low" determine that the memory is one-time programmable; however, it is apparent that in this case, the cell holding the value of "0," meets the limitation of having all "0"s.

Regarding dependent claim 6, Fasoli discloses that the one-time programming region (Fig. 2 [3a]) is programmed with certain data (column 5, lines 61-65).

As per **dependent claim 20**, it encompasses the same scope of invention as to that of claim 6 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 2, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fasoli (U.S. Patent 6,490,197 B1) in view of Applicant's Admitted Prior Art (AAPA).**

Fasoli shows all of the limitations of claim 1 and claim 18, from which claim 2 and claim 19 depend (see above rejection). Fasoli does not explicitly state reprogramming the non-volatile memory without performing an erase operation. However, Fasoli does not suggest that an erase operation must be performed prior to a reprogramming operation (column 5, lines 14-17).

AAPA teaches that FRAM, PRAM, and MRAM are non-volatile memories that are capable of reprogramming without the need for first performing an erase operation (page 2, line 3-6).

It would have been obvious to one of ordinary skill in the art at the time of the invention select FRAM, PRAM, or MRAM as the nonvolatile memory used by Fasoli for the purpose of reprogramming the memory without the need for first performing and erase operation. Further motivation to perform the above stated modification is evidented by the fact that FRAM, PRAM, and MRAM are types of non-volatile memory and Fasoli is from the same field of endeavor as classified under U.S. Cl 365 (static memories).

Allowable Subject Matter

11. **Claims 7-17** would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

With respect to **independent claim 7**, the following is an examiner's statement of reasons for allowance: There is no teaching or suggestion in the prior art to accessing a lock bit region (see claim objection) in response to a first decoding signal where the sense amplifier compares the data output from the lock bit region to generate a first comparison detecting signal, and comparing the data of the one-time programming region to generate a second comparison detecting signal, and then generating a write driver enable signal (see claim objection) in response to the first and second detecting signals.

12. **Claims 21-23** would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

With respect to **independent claim 21**, the following is an examiner's statement of reasons for allowance: There is no teaching or suggestion in the prior art to comparing the data read from a lock bit region (see claim objection) to generate a first comparison detecting signal, and comparing the data of the one-time programming region to generate a second comparison detecting signal when the first comparison detecting signal is generated, stopping the write operation when the first or second comparison detecting signal is not activated, and writing data in the one-time programming region when the one-time programming region and the lock bit region are not accessed or the second comparison detecting signal is activated.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Takata (U.S. Patent 6,469,928), Chiu et al. (U.S. Patent 6,882,577 B2), and Alva et al. (U.S. Patent Application Publication 2005/0177679 A1).

Takata shows a nonvolatile semiconductor memory device where any non-volatile memory block can be an OTP. A lock bit determines whether or not the memory block is an OTP. The semiconductor memory device also has a read/write circuit, a sensing amplifier, and a control circuit.

Chiu et al. show a chip that comprises a memory section that is divided into an on-system programmable memory and an off-chip programmable memory; where the off-chip programmable memory can be an OTP.

Alva et al. show a memory device comprising MRAM and parity circuitry. This application discloses the use of combinations of different memory technologies, e.g., OTP, SRAM, DRAM, and flash memory.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

11/20/07

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